ATTACHMENTS

i. **Page 5** of the Detailed Description

ii. **FIG. 2** of the Drawings

iii. **Pages 1 - 4** of a Restriction Requirement Mailed 09/11/2002 and stating the now Waived objections to **FIG. 2**.

AUTHORIZATION TO CHARGE FEES DUE TO THE HP PTO DEPOSIT ACCOUNT #: 08-2025

Applicant hereby authorizes any fees due to be charged to the Hewlett-Packard PTO Deposit Account Number: **08-2025**.

CONCLUSION

Based on the foregoing, the Applicants respectfully request that the PTO accept Applicants timely payment of the Issue Fee for application serial number **09/934,548**.

Respectfully submitted,

Ping Mei

Dated: October 21, 2004 By: ________________

Trueman H. Denny, III

Registration Number **44,652**

materials can be used to form the substrate 160 because of the relatively low temperature fabrication method used to produce the memory device 10.

The data lines 130 can be thin strips of semiconductor material, such as silicon. The data lines 130 can be deposited as a silicon layer over the substrate 160, which can be subsequently patterned to form the data line 130 strips. The silicon can be an amorphous silicon deposited by, for example, plasma enhanced chemical vapor deposition (PECVD). Alternatively, the silicon strips can be polycrystalline silicon, crystalline silicon, or semiconductors such as SiGe, Ge, SiC, GaAs, and organic semiconductors. The data lines 130 can have a thickness on the order of, for example, 1000 Angstroms. The thickness of the data lines 130 may vary according to the material used to form the data lines 130.

The p-channel TFTs 170 may be used as resistive load elements for the memory array 100. The p-channel TFTs 170 may be synchronized with gate line pulses to the memory cells 200, and provide power savings during idle periods for the memory device 10. The p-channel TFTs 170 can be replaced with, for example, a simple n-channel circuit, or, a resistive circuit.

The structure of the memory cells 200 is discussed in detail with reference to Figures 3A and 3B.

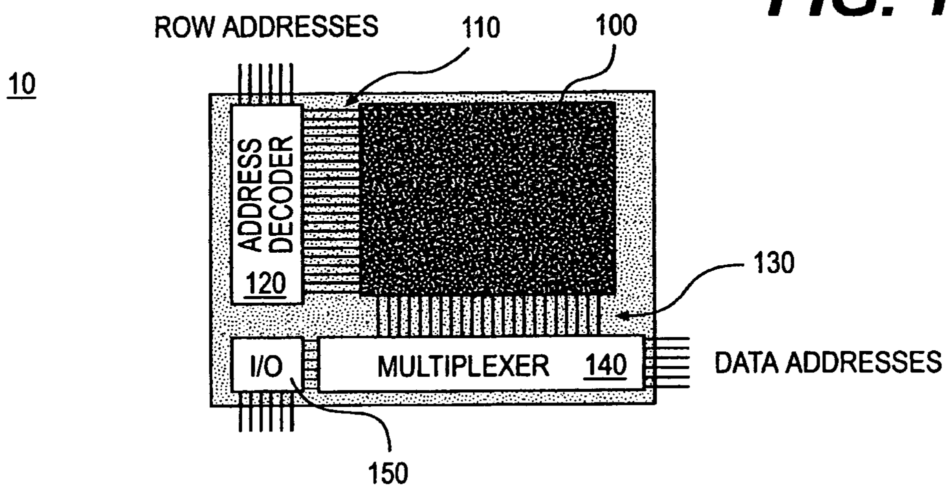
Figure 3A is a sectional view taken along the section line 3-3 in Figure 2, of a TFT memory cell 200 before a write operation. Neighboring memory cells 200 on the data line 130 are also illustrated. Figure 3B is a sectional view taken along the section line 3-3 of the memory cell 200, after a write operation.

The memory cell 200 is a three terminal transistor device. The memory cell 200 may be a thin film transistor formed at the intersection of a gate line 110 and a data line 130. The memory array 100 may therefore include a number of memory cells 200 equal to the number of intersections of the gate lines 110 and the data lines 130.

The memory cell 200 comprises a channel region 132 of the data line 130, a source region 134 of the data line 130, a drain region 136 of the data line 130, a gate insulator 211 having a gate insulator layer 212 disposed over the channel region 132 and a gate insulator layer 216 disposed over a floating gate 214, and a gate line 110 extending over the gate insulator 212. The portion of the gate line 110 contacting the gate insulator 216 serves as a gate electrode 218 for the TFT memory cell 200.

The gate insulator layers 212, 216 may be layers of dielectric material. The gate insulators 212, 216 may be separate layers on either side of the floating gate 214, as

FIG. 1


ROW ADDRESSES
110
100
10
ADDRESS DECODER
120
130
I/O
MULTIPLEXER 140
DATA ADDRESSES
150

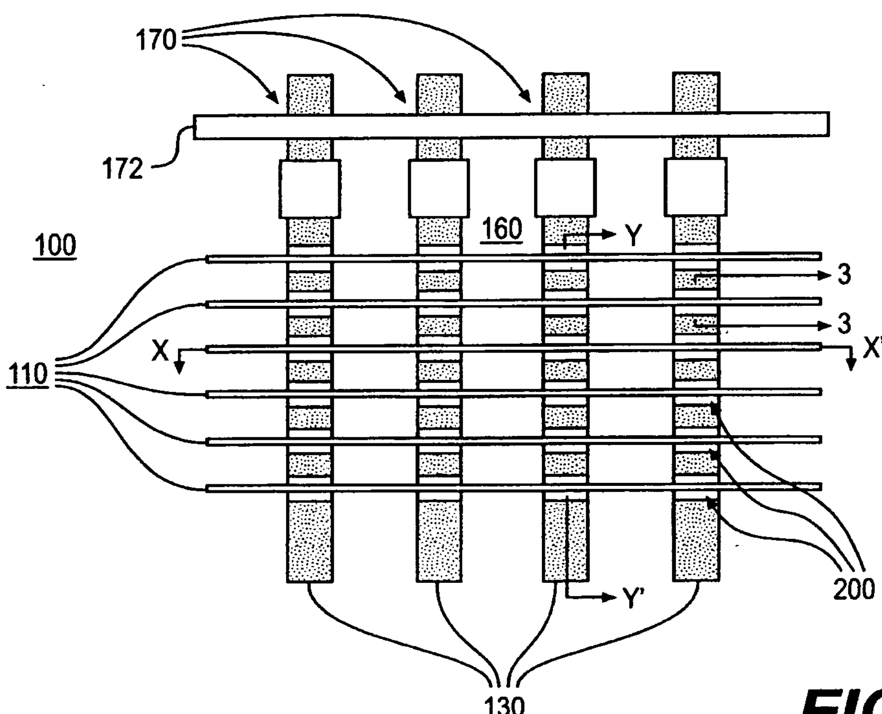

170
172
100
160
Y
3
3
X
X'
110
200
Y'
130

FIG. 2